Nepal College of Information Technology

**Unit Test**

Fall 2013

Program : BE IT Time : 2 hrs

Semester : (V) FM : 70

Subject : Computer Organization & Architecture PM : 35

* *Candidates are requested to give their answer as far as practicable in their own words.*
* *The figure in the margin indicates the full marks*
* ***Attempt ALL question***

1 a) What do you mean by ISA? Explain various types of instruction format. 7

b) Design the 16x 4 memory subsystem constructed from two 16 X2 ROM chips with

i) High Order Interleaving

ii) Low Order Interleaving. 8

2 a) Show the hardware to implement the following RTL code. 7

a) M : X 🡨X +Y

b) N :X🡨X+Y’+1

C) O :X🡨X^Y

b) Design a very simple CPU has the following instruction set and Show the RTL code for execute cycle for each Instruction 8

|  |  |  |
| --- | --- | --- |
| Instruction | Instruction Code | Operation |
| Complement | 00AAAAAA | AC🡨 AC’ |
| AND | 01AAAAAA | AC🡨AC^ M[AAAAAA] |
| JMP | 10AAAAAA | GOTO AAAAAA |
| INC | 11XXXXXX | AC🡨AC+1 |

3 a) From the above table also design the ALU and Hardwired control unit for the very simple CPU. (Chapter 4) 7

b) What do you mean by micro sequencer ?Explain with the generic micro sequencer organization 8

4 a) Describe the microinstruction format? Explain the horizontal and vertical microcode. 8

b) Explain the Assembling and compiling process with suitable examples 7

5 Write Short Notes(Any Two) 5X2=10

a) Addressing Mode

b) VHDL

c) Instruction Cycle

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